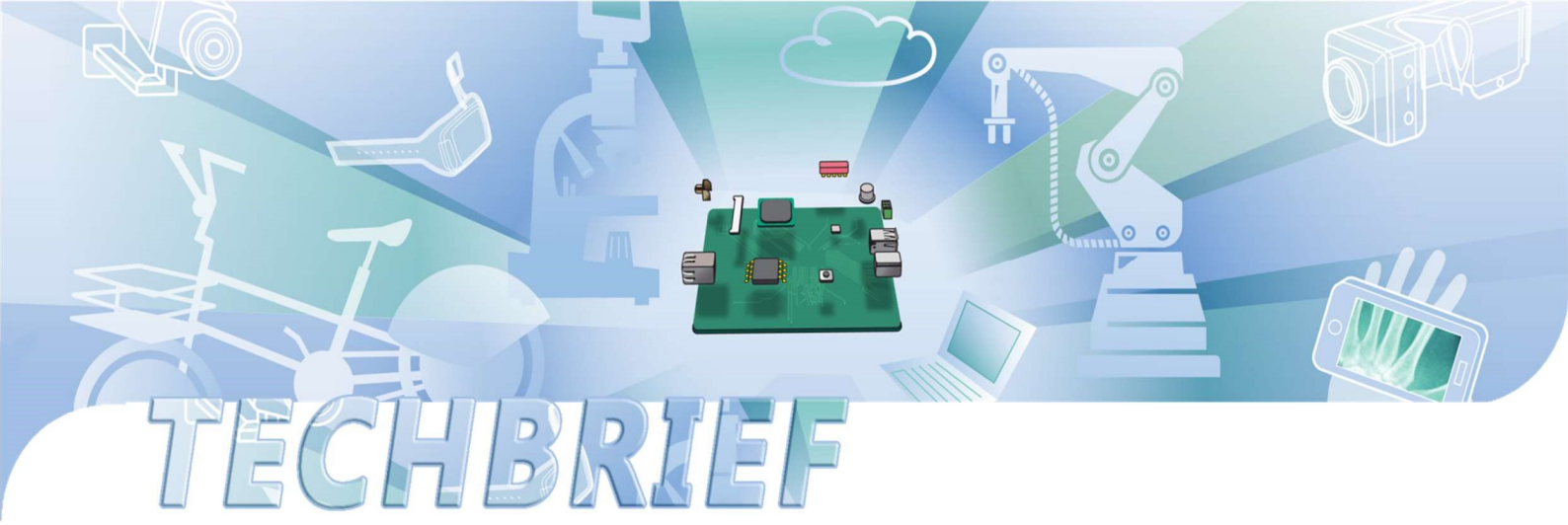
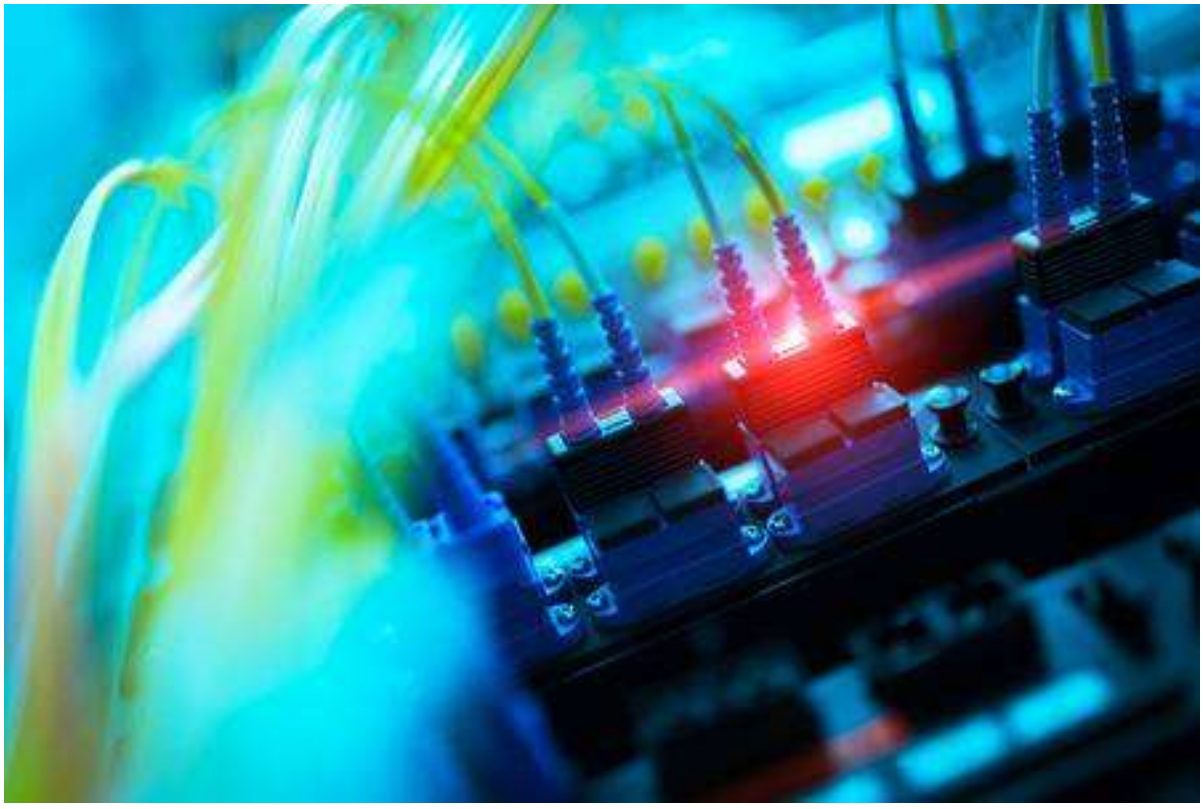


Bit-10G UDP-Ethernet

10 Gb/s full HW stack UDP/IP Transmitter/Receiver IP block for high performance data transfers from embedded Ethernet based systems



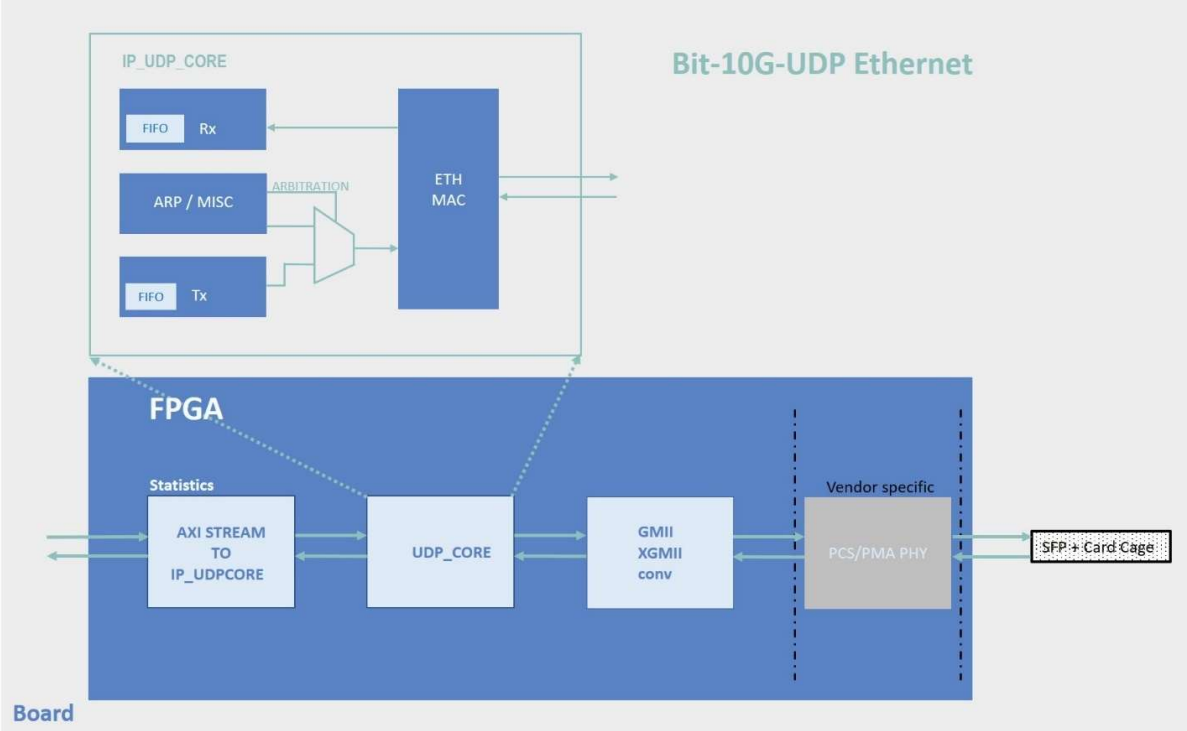
Overview

In application areas such as Data Communication and Imaging, there is a need for increased transfer speeds to handle higher resolutions and higher acquisition rates. This implies more complex solutions in terms of FPGA and board design. This IP core is a real-time offload engine where the communication is processed and accelerated in HW – all the way from UDP to Ethernet Phy. An Ethernet PHY can be integrated in the FPGA enabling a direct connect to the fiber optical SFP+ transceiver.

With data transfer near line rate at theoretical maximum throughput, it is useful for sending large amount of data to a remote PC or host.

TECHBRIEF

Bit-10G UDP-Ethernet



Features

- Transmits UDP with IP packets up to 10Gb/s, with 10G Ethernet protocol to host
- Receives UDP with IP packets up to 1Gb/s with 10G Ethernet protocol from host
- ARP-table, number of entries can be selected
- Programmable Source/Destination ports and IP/MAC/Default gateway address
- A vendor specific integrated 10 Gb/s PCS/PMA PHY enables a direct connection to SFP+ cages
- Supports the XGMII Interface to the Ethernet PHY
- Payload data is transferred via the AXI4-Stream interface
- Loopback at both AXI-Stream and XGMII interfaces are possible for debugging purposes
- PCIe header interpretation possible, for tunneling of PCIe
- Statistics counters and protocol filters
- Implemented as general VHDL code, independent of FPGA vendor
- Tested with Xilinx Ultrascale & Ultrascale+ and Intel NIC 10Gb/s Ethernet board

Deliveries

- VHDL source code (readable or encrypted) and testbench with stimuli and checkers
- PC SW driver (Windows, Linux)
- VHDL Simulation Test Benches with BitSim's Simulation Environment
- User Guide