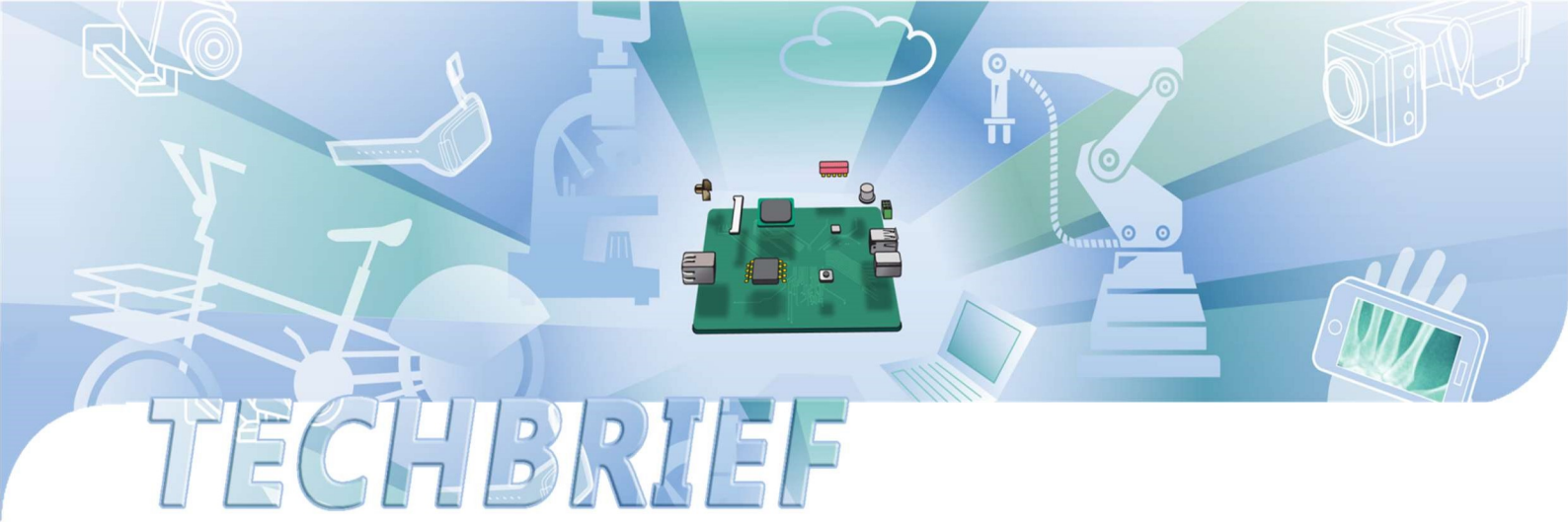
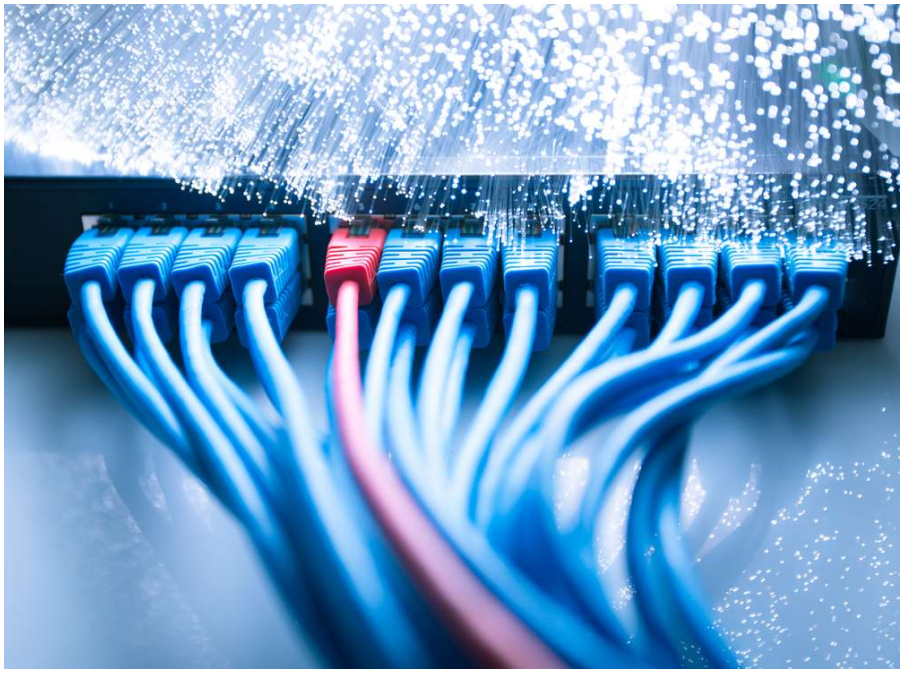


Bit-1G-UDP Ethernet

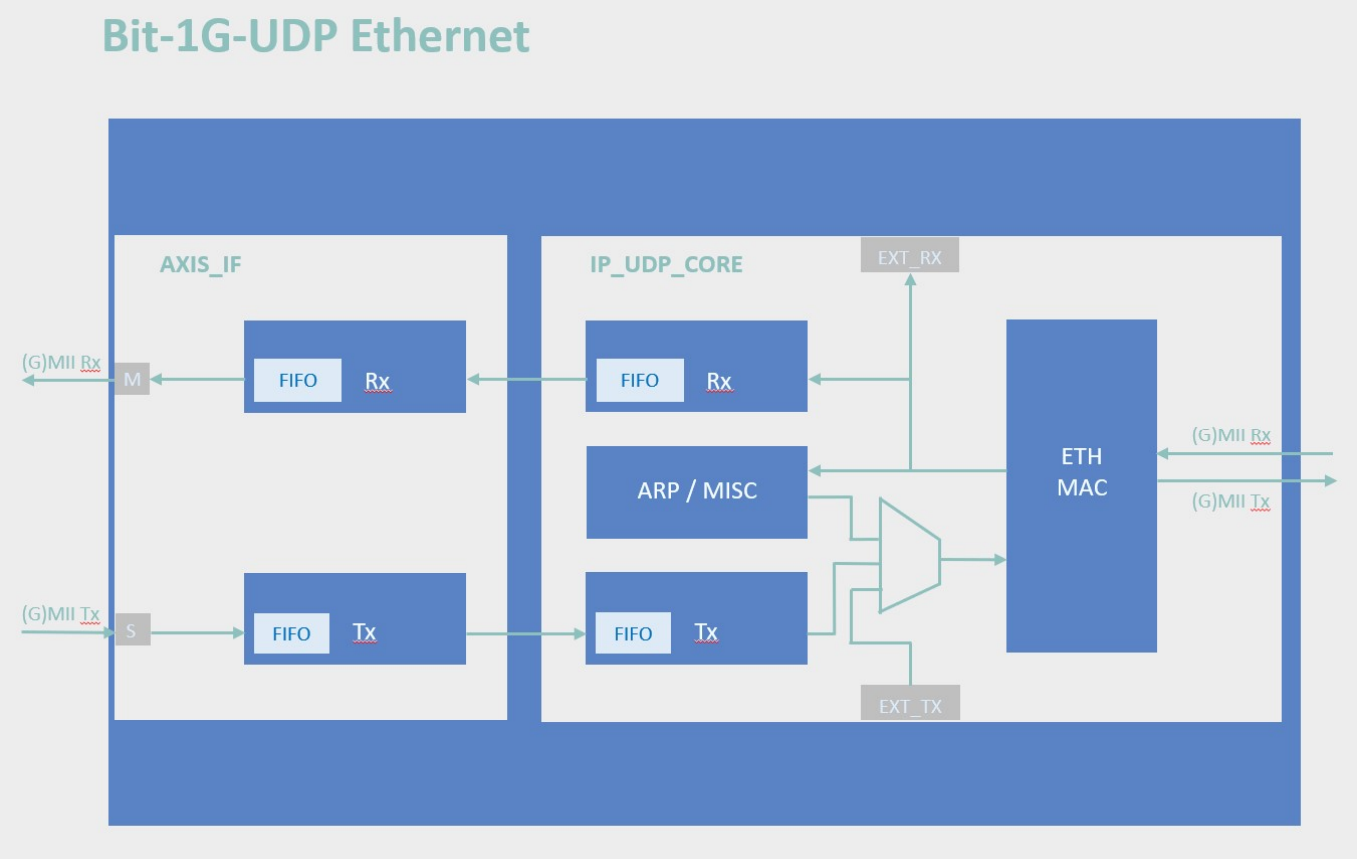
10/100 or 1000 Mb/s full HW stack UDP/IP Transmitter/Receiver IP block for high performance data transfers from embedded Ethernet based systems



Overview

In application areas such as Data Communication and Imaging, there is a need for increased transfer speeds to handle higher resolutions and higher acquisition rates. This implies more complex solutions in terms of FPGA and board design. This IP core is a real-time offload engine where all communication is processed and accelerated in HW – all the way from UDP to the Ethernet MAC.

With data transfers near line rate at theoretical maximum throughput, it is useful for sending large amount of data to a remote PC or host.



Features

- Receives and sends UDP-packets over Ethernet
- Supports 10, 100 and 1 000 Mb/s (1 Gb/s) transfer rates
- ARP-table, number of entries can be selected
- Programmable Source/Destination ports and IP/MAC/Default gateway address
- Works with standard Ethernet transceivers (PHYs) using (G)MII-interface (RGMII optional)
- Low latency (CRC on IP-header calculated on-the-fly)
- Payload data is transferred via AXI4-Stream or with a proprietary interface
- Loopback at both AXI-Stream and (G)MII interfaces are possible for debugging purposes
- PCIe header interpretation possible, for tunneling of PCIe
- Statistics counters and protocol filters
- Implemented as general VHDL code, independent of FPGA vendor
- Tested with Xilinx Zynq, Virtex-6, Virtex-5 and Marvell Ethernet PHYs 88E1512, M881111 EPHY

Deliveries

- VHDL source code (readable or encrypted) and testbench with stimuli and checkers
- PC SW driver (Windows, Linux)
- VHDL Test Benches and BitSim's Simulation Environment
- User Guide