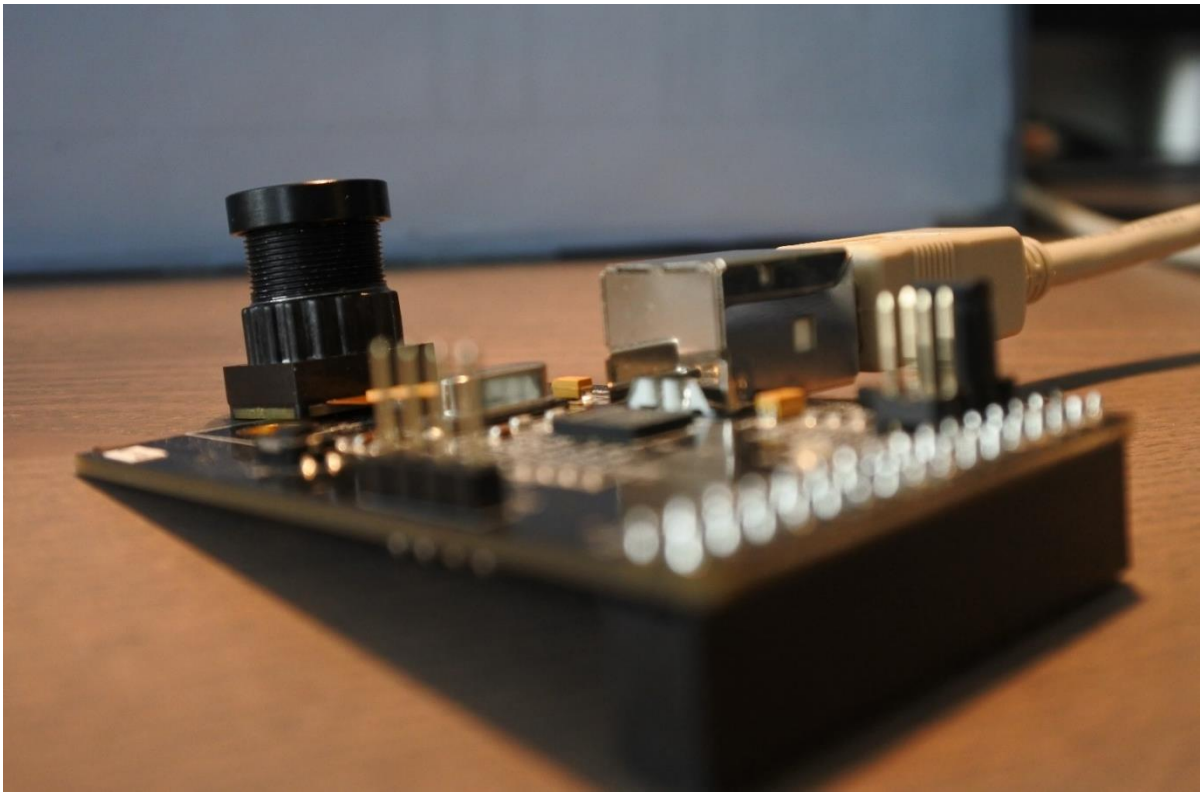
TECHBRIEF

Bit-MIPI CSI-2 Rx

A very compact, from 500 LUTs, camera sensor receiver interface converting from CSI-2 to AXI4-Stream Video standard



Overview

MIPI CSI-2, a popular high-speed serial interface specification, is often used in modern camera designs. BitSim has developed two CSI-2 cores, BitCsi2Tx and BitCsi2Rx that provides a very small footprint and cost-effective solution for your camera application. This data brief describes the receiver core, BitCsi2Rx. The design is fully configurable and is aimed for any ASIC/FPGA with camera sensors supporting the CSI-2 standard.

Features

- Fully CSI-2 compliant
- D-PHY protocol decoding included
- 1-4 data lanes + 1 clock lane
- 8/10-bit primary and RAW12/14/16 data types are supported
- Up to 2.5 Gb/s for FPGAs
- Also supports Xilinx UltraScale+ families with embedded D-PHY IOs
- AXI-4 or native control interface
- Very compact IP, only around 500 LUTs/FFs for 1 lanes/8 bit and 1000 for 4 lanes, incl the D-PHY
- Portable VHDL code with Testbench
- Supports Spartan-6/7, Artix, Zynq, MPSoC/US+ (Xilinx), Cyclone 10, MAX 10 (Intel/Altera), Polarfire (Microsemi) and others
- Demonstration platform available

A MIPI CSI-2 transmitter IP is also available from BitSim, **BitCsi2Tx.**

Deliveries

- Encrypted or readable source code (VHDL)
- VHDL testbench with stimuli and checkers and a User Guide

Licensing

- Licenses for protected or readable source code

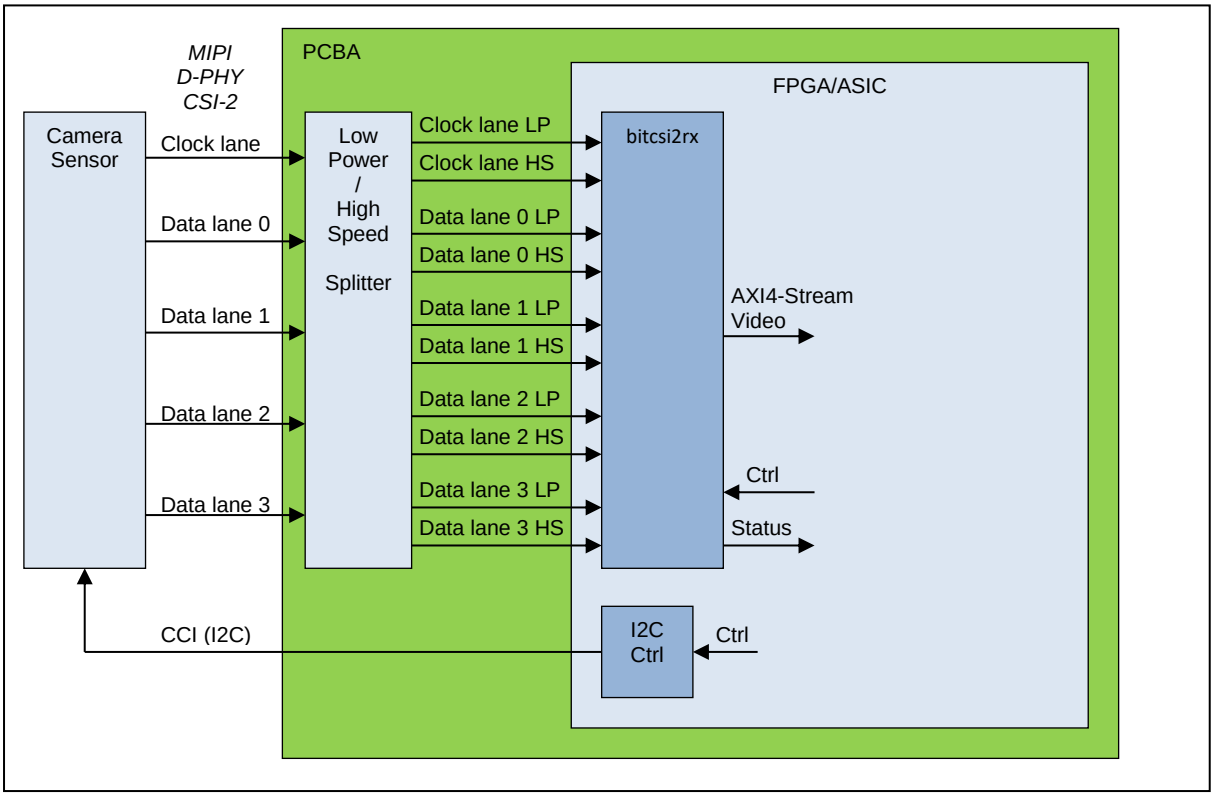


Figure 1 BitCs2Rx in a system